HEWLETT® PACKARD

GaAs IC PINFET Receiver

Technical Data

PDC2201-1.2/2.4

Features

- **Ultra High Reliability Planar InGaAs PIN Photodiode**
- **Custom GaAs IC for High Performance and Stability**
- **Transimpedance Design Optimized for High Speed Applications**
- **Gain Control**
- **1300 and 1550 Nanometer Operation**

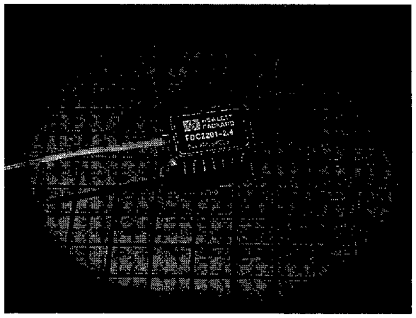
Applications

- **Optical Communication Systems Operating Up To 2.4 Gbit/s.**
- **Trunk Telecommunications**
- **Subscriber Loop**
- **Coherent Detection Receiver**

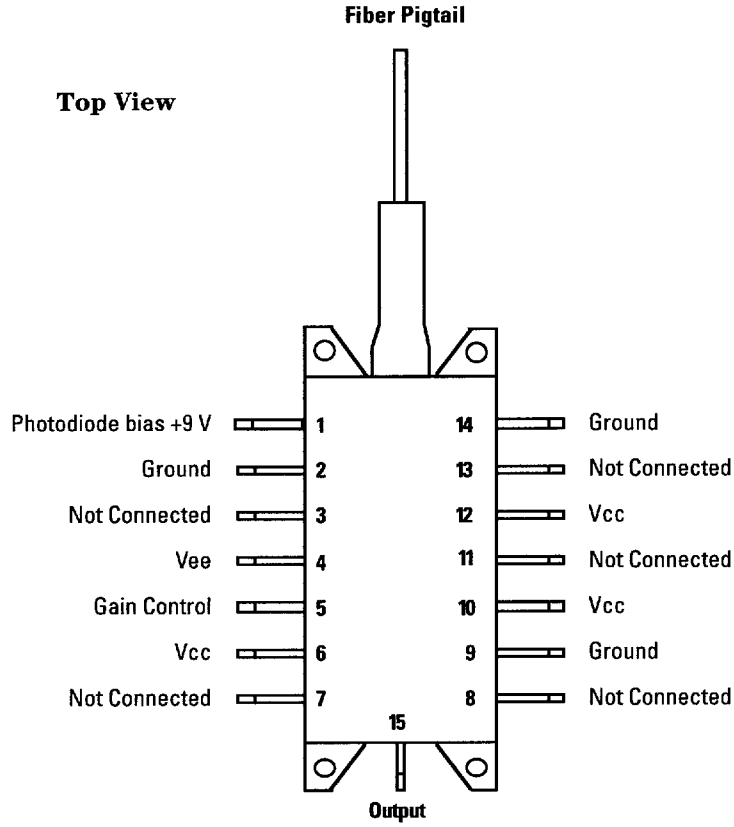
Description

PDC2201 receivers are available for data rates of 1.2 and 2.4 Gbit/s. Each variant is optimized for the particular bit rate. They serve as high sensitivity, wide dynamic range front-ends for a variety of optical receiver applications.

The planar PIN InGaAs photodiode provides excellent electro-optic performance and state of the art reliability. The high speed FET amplifiers are based on 0.5 µm GaAs circuits. The receiver is packaged in a 15 pin flatpack suitable for surface mounting, with a 50 Ohm output pin on the package end.



Connection Diagram



Pin Descriptions

Pin 1 Photodiode Bias +9 V:
+9 Volt, photodiode bias, current dependent upon incoming light level, internally bypassed with 100 pF chip capacitor.

Pins 2, 9, 14 Ground:
These pins are to be connected to the system ground.

Pins 3, 7, 8, 11, 13 Not Connected:
No internal connection.

Pin 4 Vee:
-5.2 Volt, negative supply pin for first stage output buffer, 6-8 mA nominal current, internally bypassed with 100 pF chip capacitor.

Pin 5 Gain Control:
Internally biased at +1 Volt (maximum gain), controls second stage gain. Internal circuit consists of series 100 Ohm resistor with 1000 pF shunt capacitor to ground.

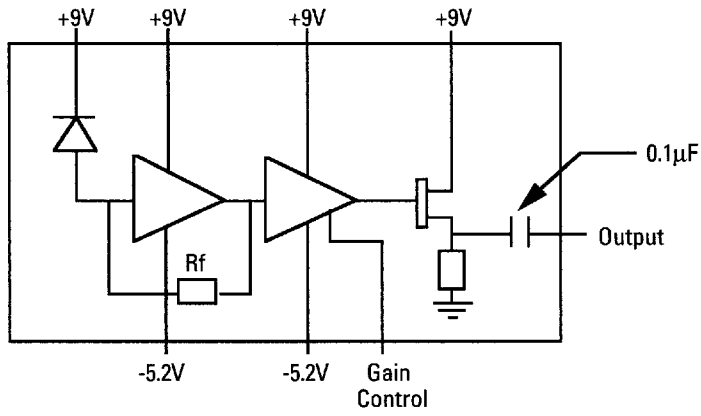
Pin 6 Vcc:
+9 Volt, output buffer stage supply, 12 mA nominal supply current, internally bypassed with 100 pF chip capacitor.

Pin 10 Vcc:
+9 Volt, gain stage supply pin, 15 mA nominal current, internally bypassed with 100 pF chip capacitor.

Pin 12 Vcc:
+9 Volt, transimpedance stage supply pin, 18 mA nominal current, internally bypassed with 100 pF chip capacitor.

Pin 15 Output:
Signal Output Pin, connected to I.C. through 0.1 µF chip capacitor.

Block Diagram



Functional Description

The PDC2201 receiver family consists of standard PINFET style optical receivers optimized for data rates of 1.2 and 2.4 Gbit/s. The optical fiber input is aligned to a very high reliability planar InGaAs PIN photodiode offering a high fiber coupled responsivity and very low dark current (less than 5 nA). The photodiode is connected to a high performance transimpedance FET amplifier integrated on a custom GaAs IC. This amplifier is designed with an output impedance of 50 Ohms and is internally capacitively coupled to the device output pin via a 0.1 µF capacitor.

It is possible for the user to alter the gain of the amplifier circuit by applying a control voltage to the Gain Control pin. (See page 4).

This circuit configuration offers very high product reliability (500,000 hours MTTF at 25°C).

Electrical Performance

The circuit requires a positive supply of +9 Volt, which is used to power the GaAs circuit and also bias the photodiode.

The circuit also requires a negative supply of -5 Volt and good electrical ground integrity for optimum sensitivity.

The photodiode cathode is connected to a separate package pin to enable the user to monitor the detector photocurrent.

The analog electrical output gives a peak to peak output voltage signal, which is proportional to the incident optical input power for inputs up to the maximum optical input power. Above this power the output voltage swing tends to limit, and the amplifier circuit saturates giving rise to pulse width distortion.

Input power up to 10 mW can be applied without damaging the device.

Layout Considerations

In order to optimize the device sensitivity at high bit rates, careful attention should be paid to the connection methods used when configuring the device. It is recommended that the following steps should be taken:

a) The device case is internally connected to ground, so it should be mounted with good contact to the metalized system ground on the PCB. The drilled flanges on the package can be soldered, riveted or bolted to the ground plane of the system ground as a further improvement.

b) In order to damp the resonance due to lead inductances and decoupling capacitors, it is recommended that the device power supplies be decoupled with a series combination of 22 Ω plus 0.1 µF (the resistance reducing the Q of the decoupling network).

c) The device operates in a 50 Ω system. It is recommended that the electrical output is routed to subsequent signal processing stages using a microstrip or coplanar line.

Function Description Contd.

Gain Control

The high electrical gain of the PDC2201 can be reduced for applications where high optical input power is used. This is done using the Gain Control pin. Pin 5 is internally connected to a gain control element on the GaAs IC. If left unconnected, it will self bias to approximately +1.5 Volt with the circuit in its maximum gain configuration. The circuit gain can be reduced by applying an external dc control voltage to this point, and taking it more negative.

There is little reduction in gain in taking this point from +1.5 Volt to GND, so it is recommended that a unipolar supply is used, the gain reducing in a non-linear fashion by approximately 30 dB on taking the gain control point to the negative rail.

Alteration of the circuit gain does not significantly affect the shape of the device frequency response.

Measurement Techniques

Device sensitivity is quoted for a 10^{-11} bit error rate and is measured by modulating a 1.3 μm laser source at the specified data rate with an NRZ 2^{15} -1 PRBS. The laser source is coupled to the device via a 2 km length of single mode fiber (to modestrip and eliminate reflections) and an optical attenuator. The device signal output is coupled, via an amplifier/regenerator and a filter with -3 dB point at 0.7 of the bit rate, to an error rate test set.

Packaging

The circuit is mounted in a hermetic 15 pin flatpack to facilitate ease of mounting with coplanar/microstrip connections.

Adequate heatsinking must be provided to ensure that the case temperature does not exceed +85°C in operation.

Performance Specifications (Note 6)

PDC2201-1.2

Parameter	Minimum	Typical	Maximum	Units	Note
Bit Rate	-	1200	-	Mbit/s	-
-3 dB Frequency	-	650	-	MHz	1
Sensitivity	-	-	-30	dBm	2
Output Signal at Sensitivity	-	15	-	pk-pk mV	3
Responsivity	-	10.2	-	kV/W	3
Maximum Optical Power	-	-8.0	-	dBm	4

PDC2201-2.4

Parameter	Minimum	Typical	Maximum	Units	Note
Bit Rate	-	2400	-	Mbit/s	-
-3 dB Frequency	-	1700	-	MHz	1
Sensitivity	-	-	-25	dBm	2
Output Signal at Sensitivity	-	12	-	pk-pk mV	3
Responsivity	-	3.7	-	kV/W	3
Maximum Optical Power	-	-8.0	-	dBm	4

Parameter	Minimum	Typical	Maximum	Units	Note
Wavelength	1100	-	1650	nm	-
Output Impedance	48	50	52	Ohms	-
Vcc Supply Voltage	-	9	-	V	-
Current	-	60	-	mA	-
Vee Supply Voltage	-	-5.2	-	V	-
Current	-	6	-	mA	-
Total Power	-	600	700	mW	-
Fiber Length	0.4	1	-	meter	5
MTTF (@ 25°C case temp)	-	500,000	-	hours	-

Maximum Ratings

Parameter	Minimum	Typical	Maximum	Units	Note
Case Operating Temperature	-20	-	85	°C	-
Storage Temperature	-40	-	85	°C	-
Optical Input Power	-	-	10	mW	-
Supply Voltage Vcc	-0.5	-	9.5	V	-
Vee	-5.5	-	0.5	V	-

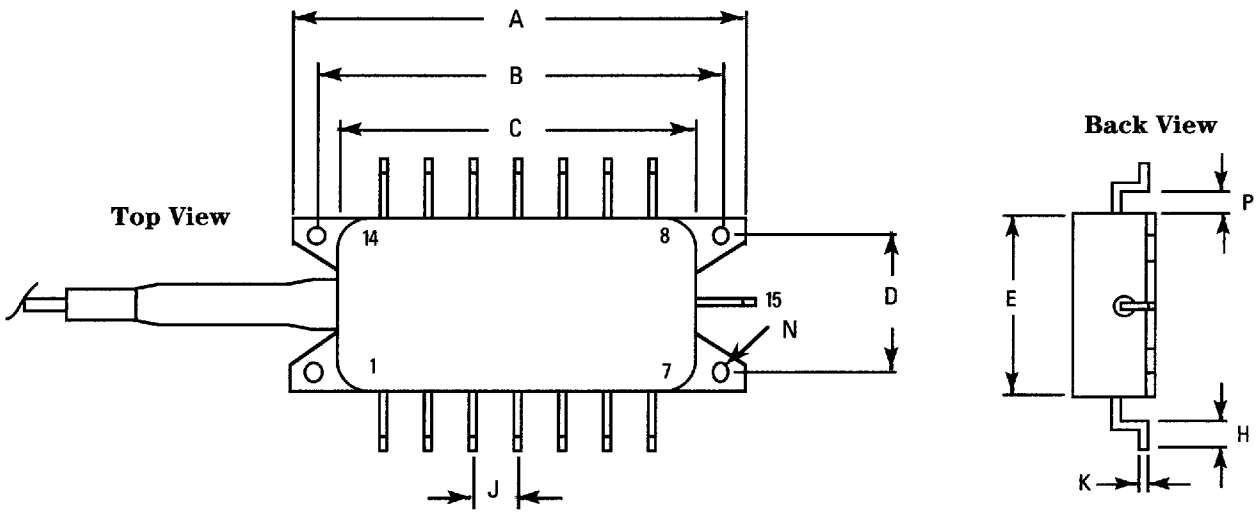
Notes:

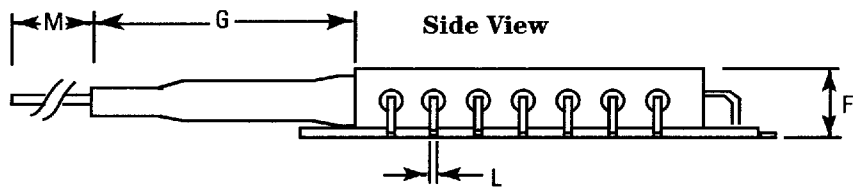
1. Typical value given. If minimum bandwidth is required for analog applications, please specify at time of order.
2. Measured at 1300 nm wavelength, 10^{-11} BER, 100% modulation depth, 2^{15} -1 pseudo-random pattern.
3. Responsivity with gain control set for maximum gain.
4. For 10^{-11} BER.
5. Fiber specifications - 50/125 core/cladding diameter 900 µm outside diameter silicone/nylon tight jacket temperature rated at 85°C.
6. At 25°C unless otherwise noted.

Drawing Dimensions

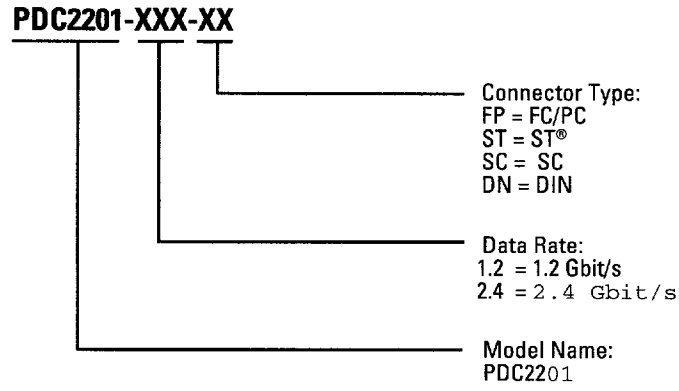
DIM	MIN	NOM	MAX
A	25.26	-	25.46
B	-	23.10	-
C	20.45	-	20.95
D	-	10.70	-
E	12.60	-	12.80
F	6.03	-	6.39
G	-	30	-
H	0.75	-	1.25
J	-	2.54	-
K	-	0.30	-
L	-	0.38	-
M	400	-	-
N	-	1.00	-
P	-	1.00	-

All dimensions in mm





Ordering Information



Allowable Part Numbers:
PDC2201-1.2-FP
PDC2201-1.2-ST
PDC2201-1.2-SC
PDC2201-1.2-DN
PDC2201-2.4-FP
PDC2201-2.4-ST
PDC2201-2.4-SC
PDC2201-2.4-DN

Handling Precautions

1. The PDC2201 can be damaged by current surges or overvoltage. Power supply transient precautions should be taken.
2. Normal handling precautions for electrostatic sensitive devices should be taken.

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